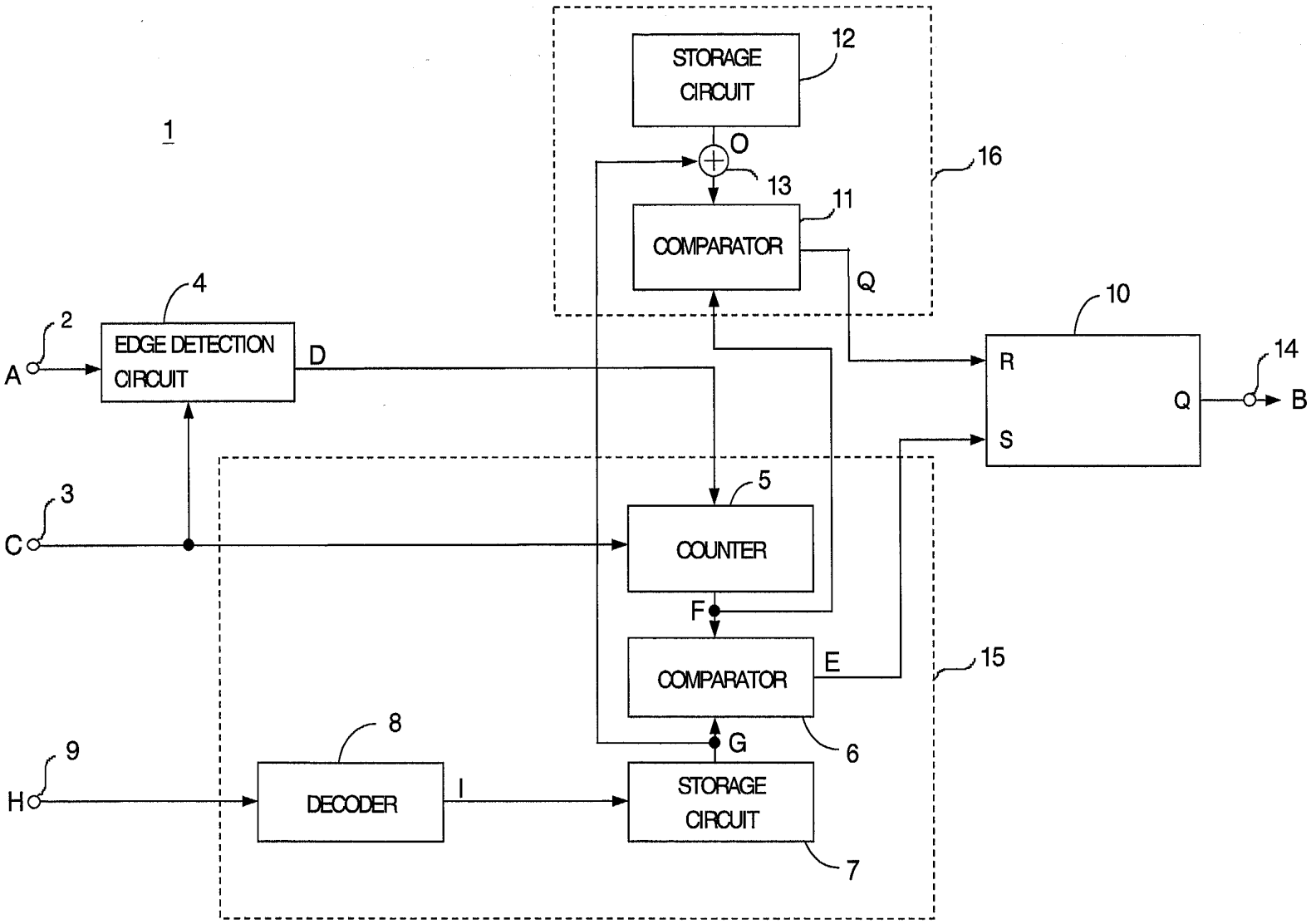
1
STORAGE CIRCUIT
12
O
13
16
COMPARATOR
11
Q
4
2
A
EDGE DETECTION CIRCUIT
D
10
R
Q
14
B
S
3
C
5
COUNTER
F
COMPARATOR
E
15
8
9
H
DECODER
I
G
6
STORAGE CIRCUIT
7

FIG. 1

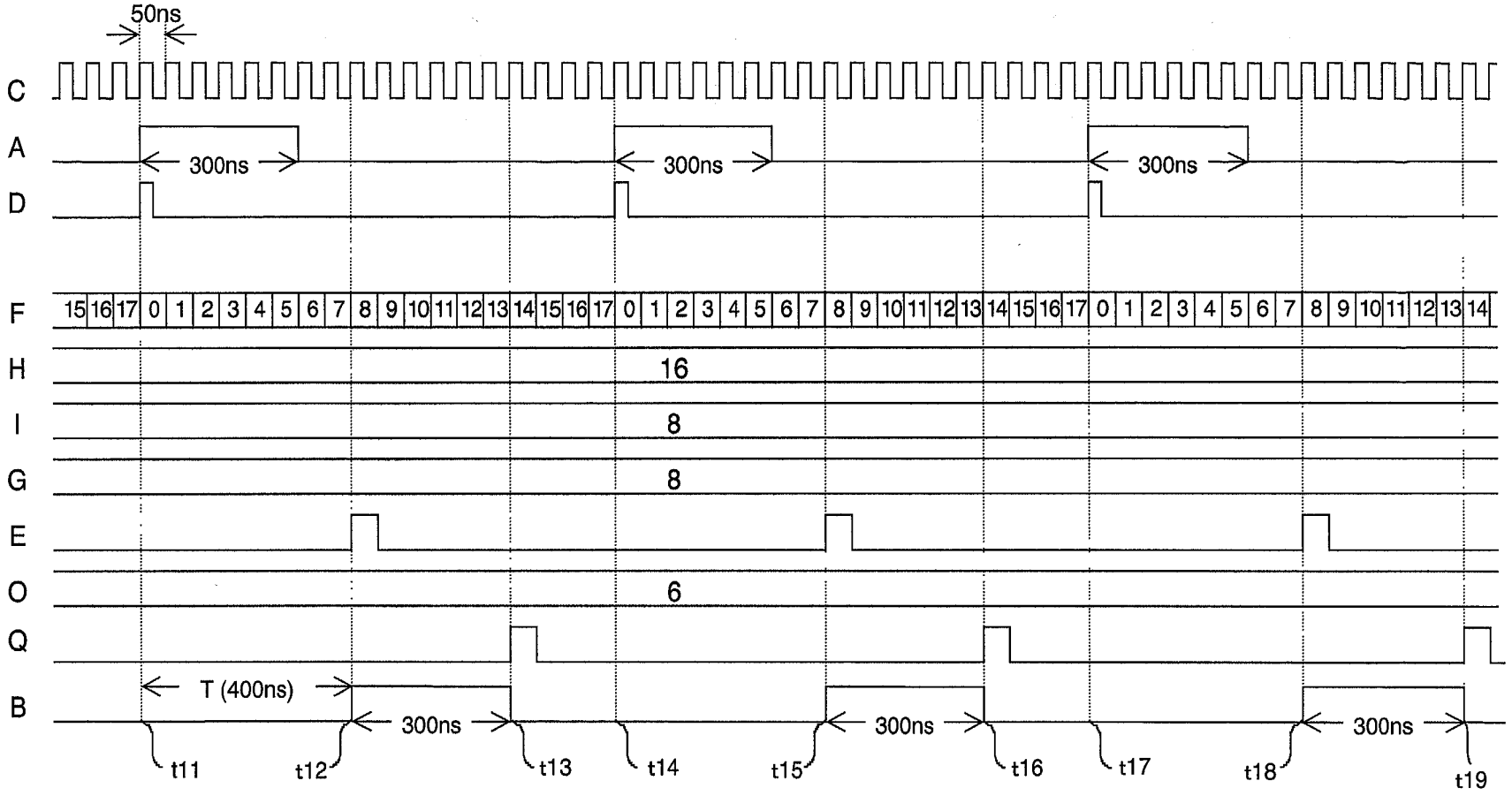
50ns
C
A
D
F
H
I
G
E
O
Q
B
300ns
300ns
300ns
15 16 17 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14
16
8
8
6
T (400ns)
300ns
300ns
300ns
t11
t12
t13
t14
t15
t16
t17
t18
t19

FIG. 2

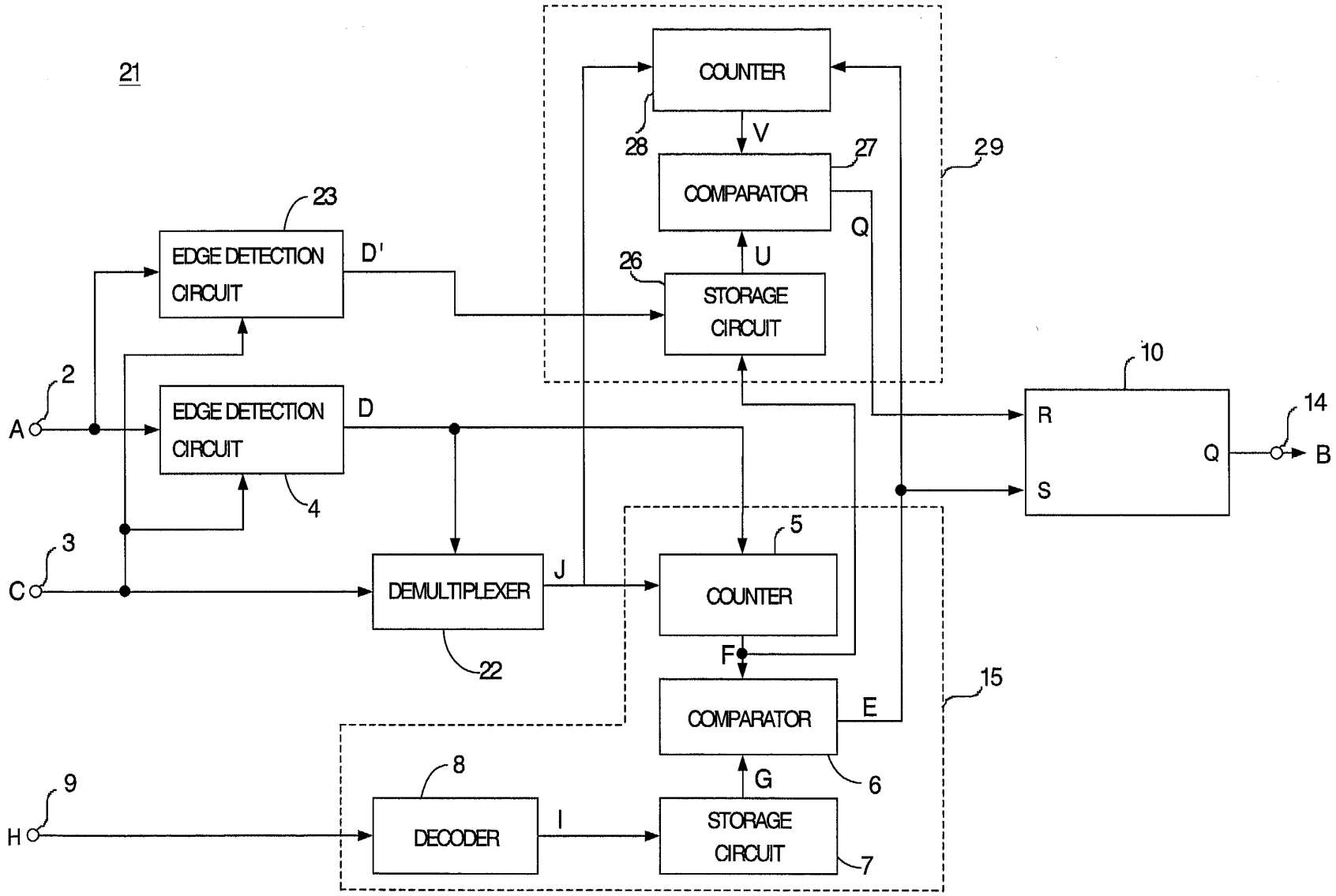
21
COUNTER
28
V
27
29
COMPARATOR
Q
23
EDGE DETECTION CIRCUIT
D'
26
U
STORAGE CIRCUIT
10
2
A
EDGE DETECTION CIRCUIT
D
4
R
Q
14
B
S
3
C
DEMULTIPLEXER
J
5
COUNTER
22
F
15
COMPARATOR
E
6
8
9
H
DECODER
I
G
STORAGE CIRCUIT
7

FIG. 3

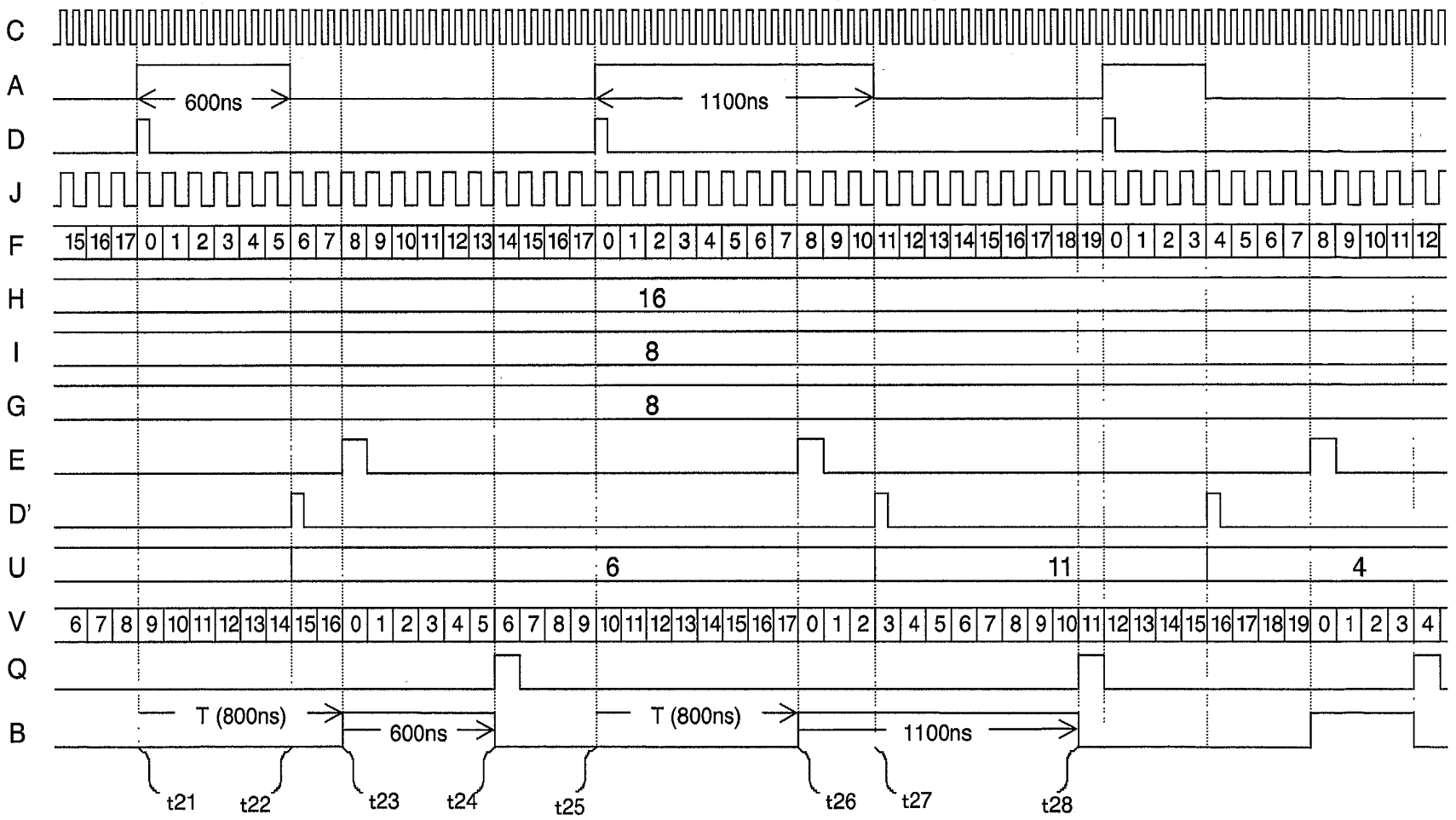
C
A
D
J
F
H
I
G
E
D'
U
V
Q
B
600ns
1100ns
16
8
8
6
11
4
T (800ns)
600ns
T (800ns)
1100ns
t21
t22
t23
t24
t25
t26
t27
t28

FIG. 4

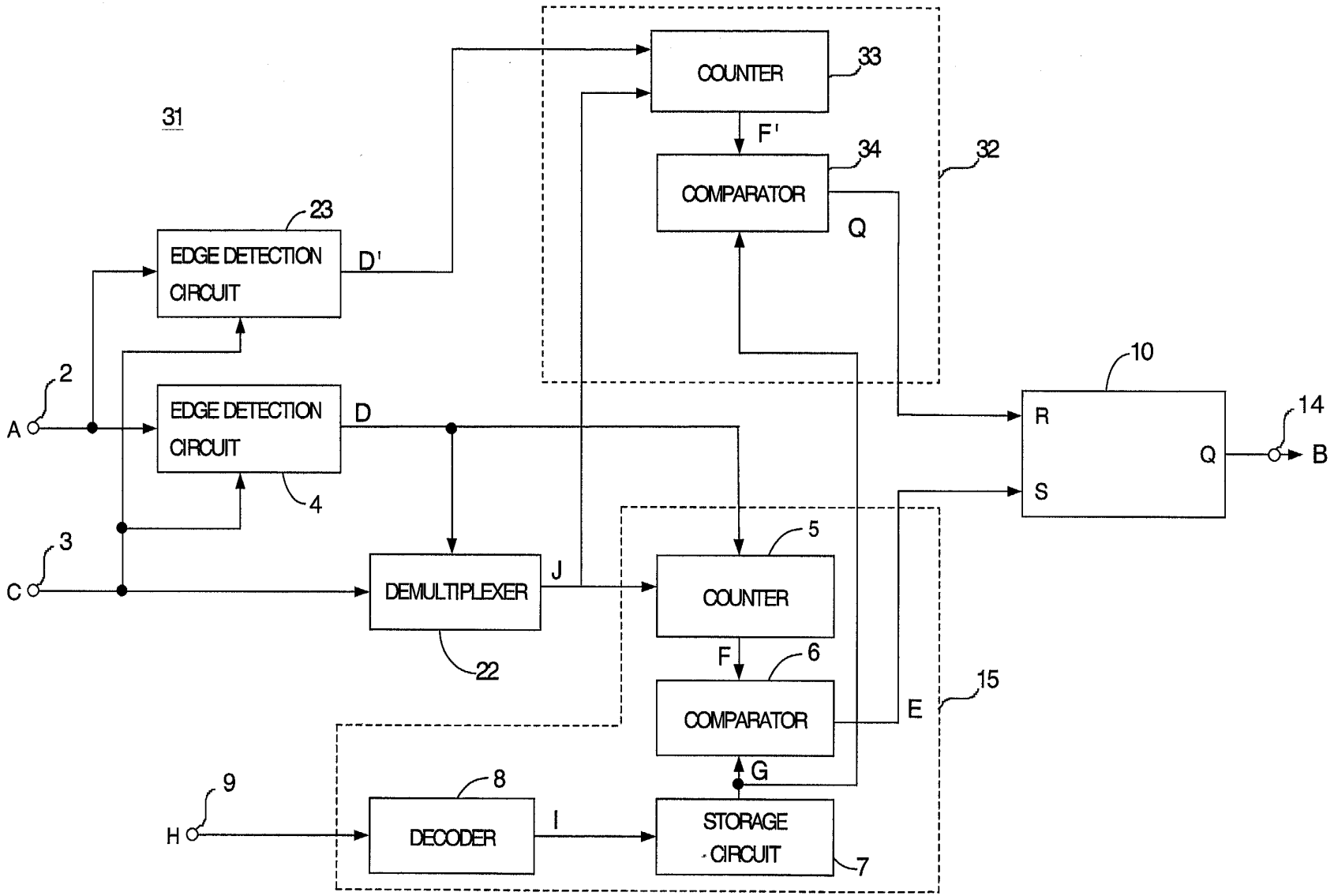

FIG. 5

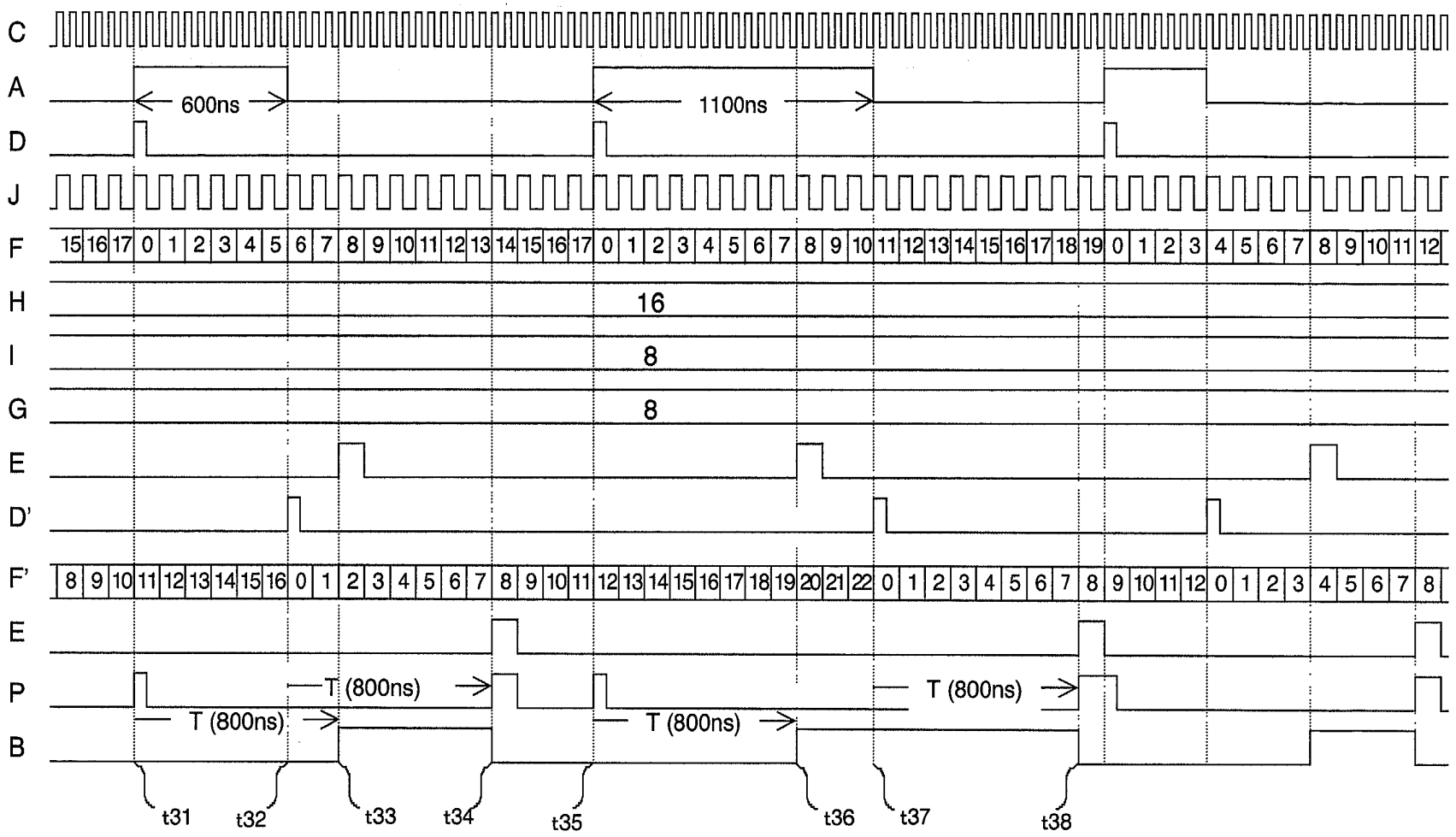

FIG. 6

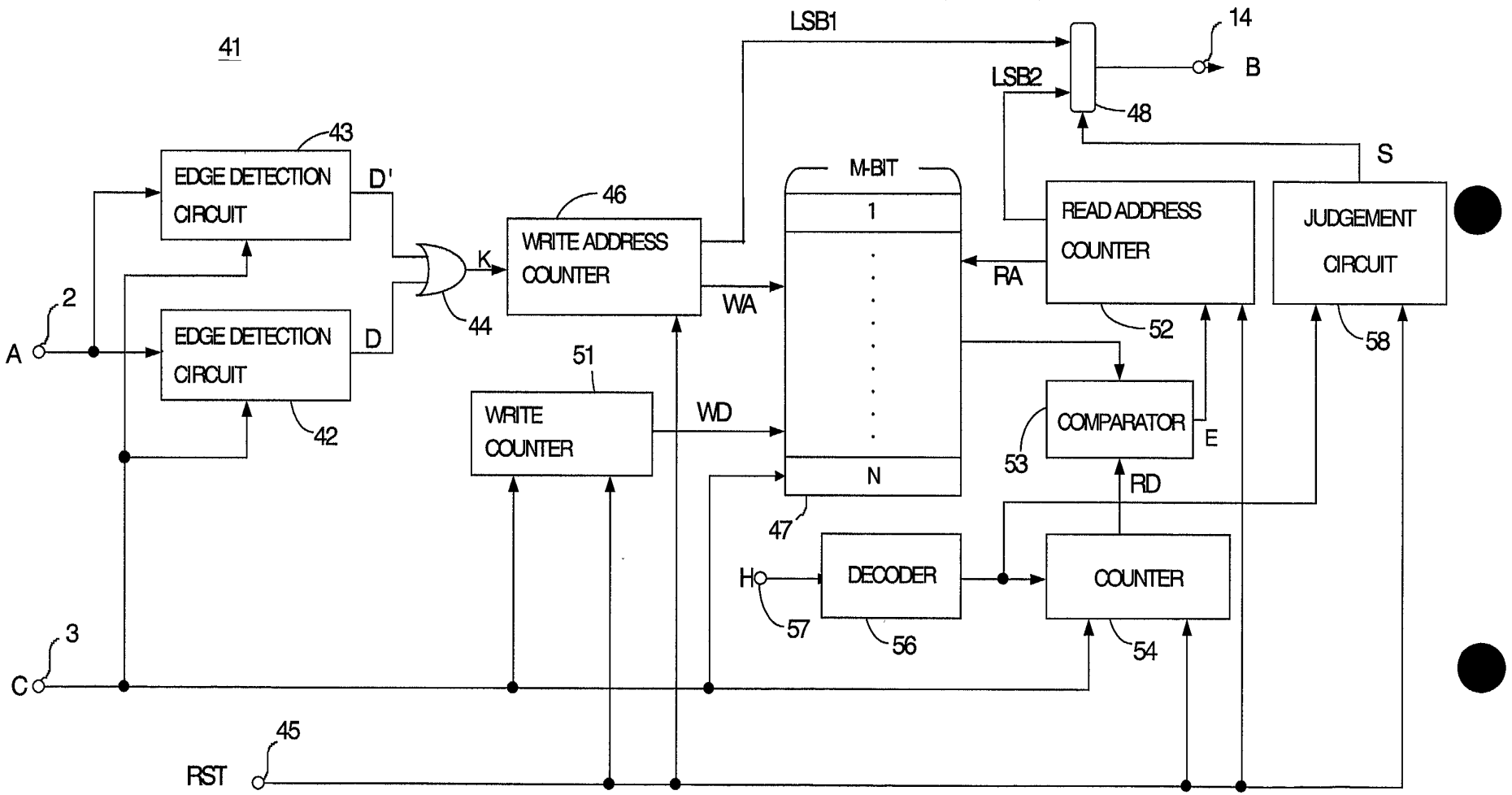

FIG. 7

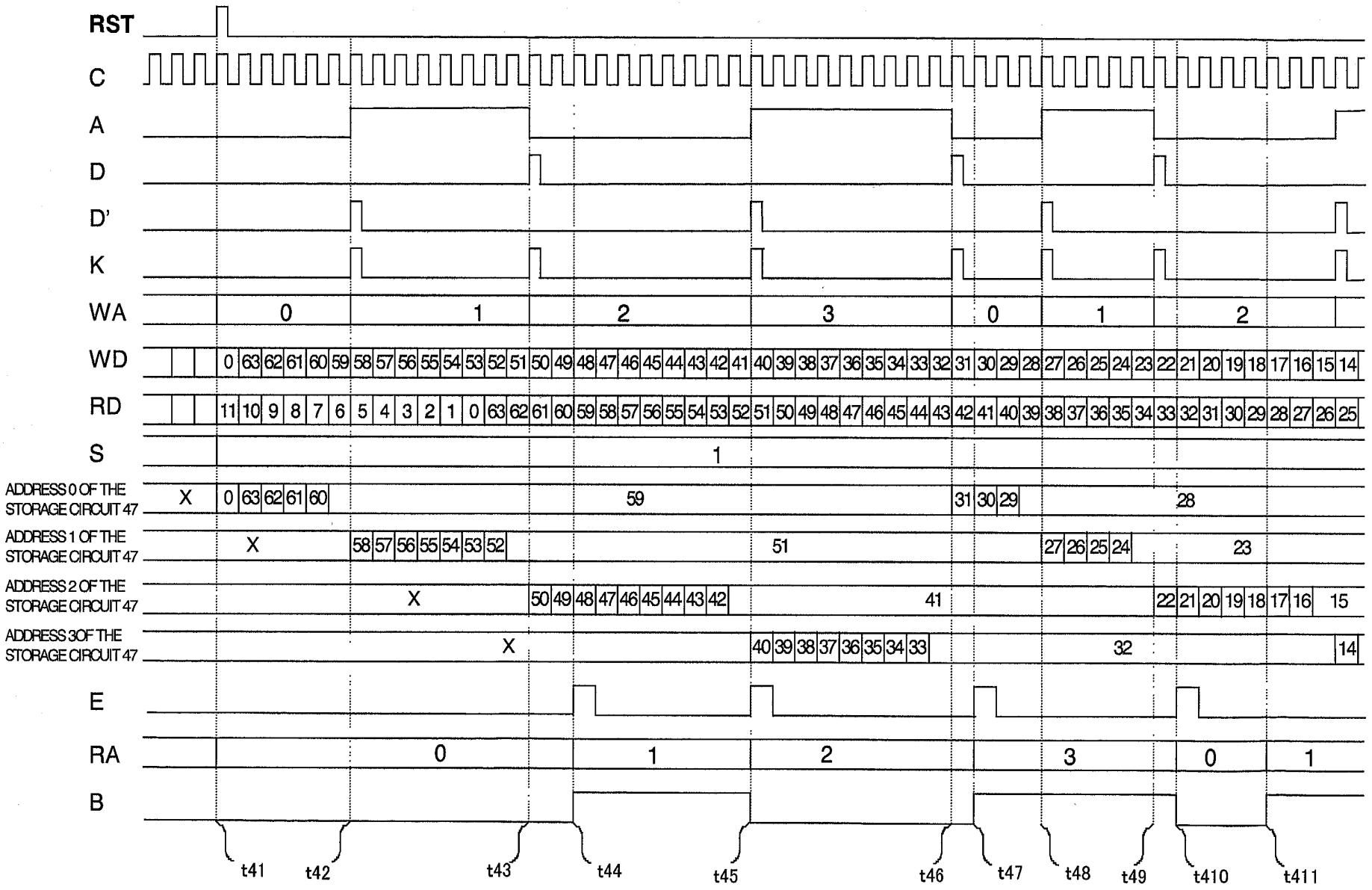
RST
C
A
D
D'
K
WA
WD
RD
S
ADDRESS 0 OF THE STORAGE CIRCUIT 47
ADDRESS 1 OF THE STORAGE CIRCUIT 47
ADDRESS 2 OF THE STORAGE CIRCUIT 47
ADDRESS 3OF THE STORAGE CIRCUIT 47
E
RA
B
t41
t42
t43
t44
t45
t46
t47
t48
t49
t410
t411

FIG. 8

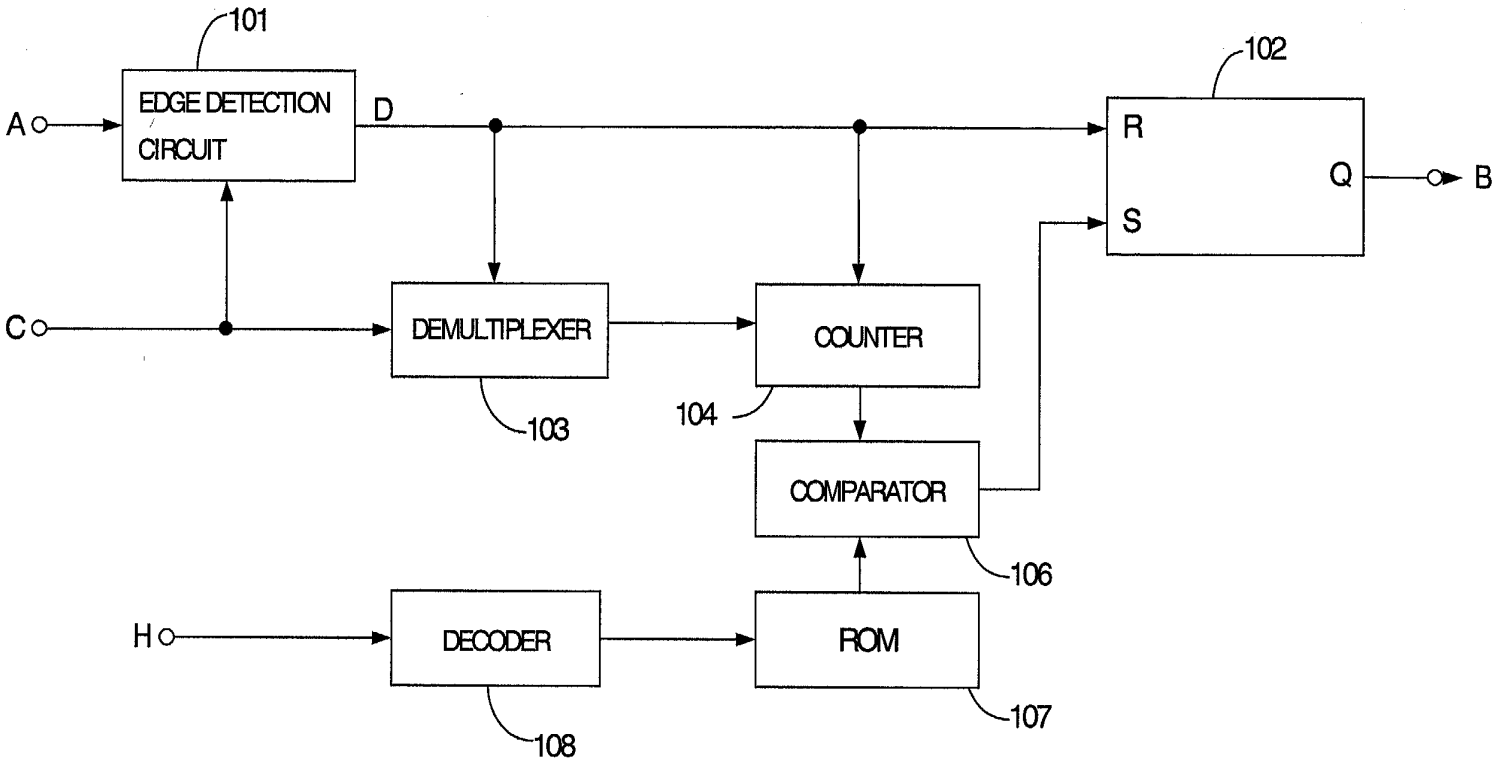

FIG. 9 (PRIOR ART)

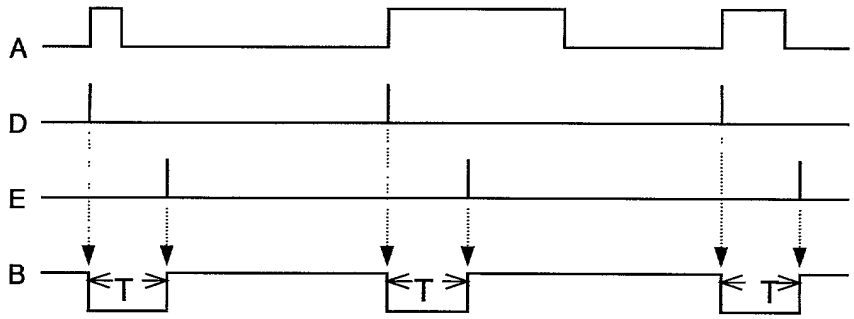

FIG. 10 (PRIOR ART)

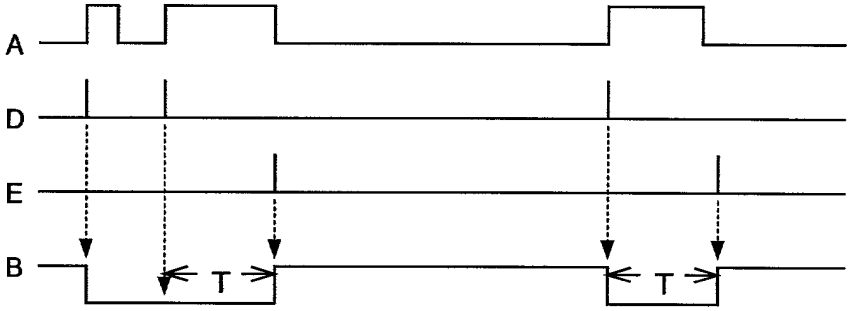

FIG. 11 (PRIOR ART)